神匠創意股份有限公司

產品說明書

產品類別：GS GaN FET

產品名稱：GS GaN FET(650 V GaN FET)

Part No.GS75H250G4C

Part No.GS75H250G4LGS

新竹縣竹東鎮中興路 **4** 段 **195** 號 育成中心 **52** 館 **328**
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sales@godsmith.com.tw

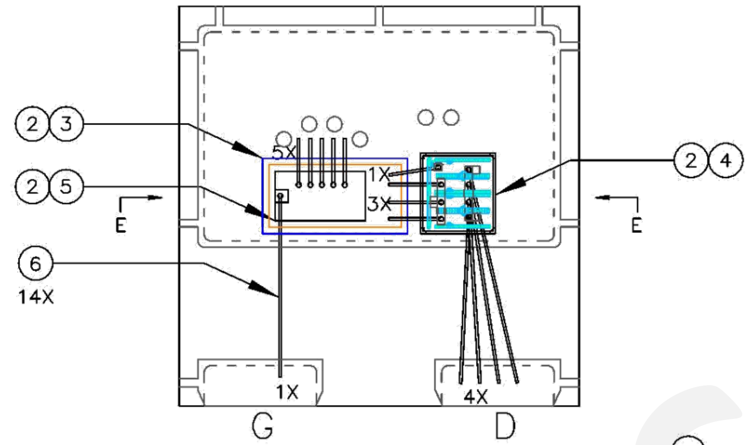
2022 年 **5** 月 **20** 日

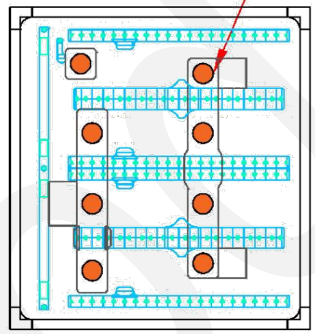
概說：

- The GS GaN FET 是以 GS Gen IV platform 製造的 gallium nitride (GaN)FET。GS Gen IV platform 技術著重在 epi 磊晶的均勻性、穩定性和較大的可用面積。
- 其中 GS75H250G4C 是裸晶(die)，GS75H250G4LGS 是將 GS75H250G4C 以 8x8 PQFN 封裝的完成品。
- 在使用上高度相容於市場常用的 TP65H300G4LSG GaN FET，可以直接轉換使用。
- 詳細資訊及應用範例見產品說明書及產品應用設計指南。

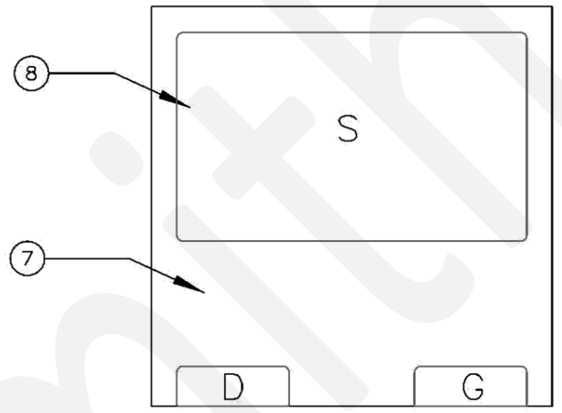
GS75H250G4C

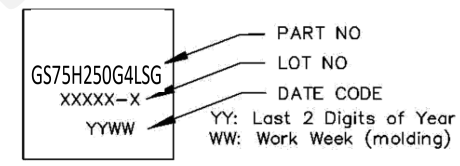
封裝說明書





D pad opening was enlarged. Target all four balls at center like this to avoid bonding on via.





TOP MARKING (LASER)

Eng only

REFERENCE DOCUMENTS:
1. TEST PROGRAM SPECIFICATION: N/A
2. PACKAGE OUTLINE DRAWING No: POD-00X
3. MARKING SPECIFICATION: SUPPLIER SPEC

Notes: Assembly
1. Clear saw street width 07G37: 100um, SiFET: 80um
2. Metallurgy of bond pads: SiFET: AlSi, HEMT: AlCu
3. Bond pad size: SiFET: G 8mil x 8mil, 07G37: S: 6mil x 36mi, Rb: 6mil x 6mil, D: 6mil x 36mil
4. HEMT ball bonding ball location, please try to distribute like above insert drawing. This is to avoid ball hitting via directly.

NOTES, PACKING
1. T&R

"Company confidential. Not controlled if printed."

ITEM	REFERENCE NUMBER	DESCRIPTION	QTY
8	xxxxxx	Tin Plating 100%	A/R
7	xxxxxx	Mold Compound	A/R
6	xxxxxx	Wire, Au PCC Cu. (2 mils)	14
5	xxxxxx	Si FET (1.80mmx0.99mmx0.20mm, 71milx39milx8mil)	1
4	07G37	HEMT (1.5mmx1.61mmx0.38mm, 59milx63milx15mil)	1
3	xxxxxx	Carrier (2.9mmx1.51mmx0.25mm, 114milx59milx10mil)	1
2	xxxxxx	84-1LMISR4 Epoxy	A/R
1	xxxxxx	LF	1

PQFN 8mmx8mm POD GS75H250G4LSG Assy G D

B/D SCALE	SHEET	DRAWING NO.	VER.
1:1	1/1	Eng000000	1

GS75H250G4LGS

成品規格書

GS75H250G4LSG

650V SuperGaN® FET in PQFN (source tab)

Description

The GS75H250G4LSG 650V, 240 mΩ gallium nitride (GaN)FET is a normally-off device using GS Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

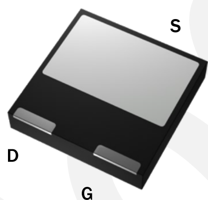
The GS Gen IV GaN platform uses advanced epi technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

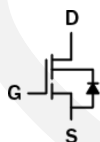
Product Series and Ordering Information

Part Number	Package	Package Configuration
GS75H250G4LSG-TR*	8x8 PQFN	Source

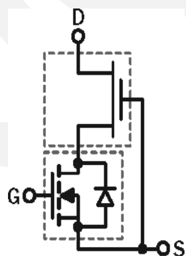
* "-TR" suffix refers to tape and reel. Refer to AN0012 for details.

GS75H250G4LSG
PQFN
(top view)





Cascode Schematic Symbol



Cascode Device Structure

Features

- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)}$ production tested
- Robust design, defined by
  - Intrinsic lifetime tests
  - Wide gate safety margin
  - Transient over-voltage capability
- Enhanced inrush current capability
- Very low Q_{RR}
- Reduced crossover loss

Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting

Key Specifications	
V_{DSS} (V)	650
$V_{DSS(TR)}$ (V)	800
$R_{DS(on)}$ (mΩ) max*	312
Q_{RR} (nC) typ	23
Q_G (nC) typ	9.6

* Dynamic $R_{DS(on)}$; see Figures 18 and 19

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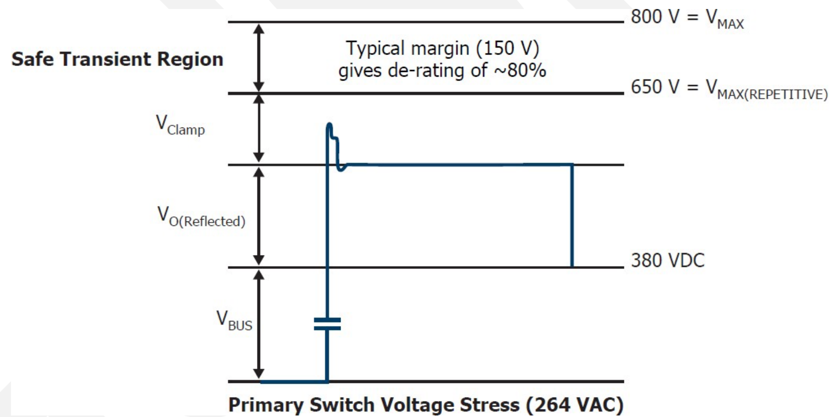
Absolute Maximum Ratings (T_c=25°C unless otherwise stated.)

Symbol	Parameter		Limit Value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)		650	V
$V_{DSS\,(TR)}$	Transient drain to source voltage [a]		800	
V_{GSS}	Gate to source voltage		±18	
P_D	Maximum power dissipation @T_C=25°C		21	W
I_D	Continuous drain current @T_C=25°C [b]		6.5	A
	Continuous drain current @T_C=100°C [b]		4.1	A
I_{DM}	Pulsed drain current (pulse width: 10μs)		30	A
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage temperature		-55 to +150	°C
T_{SOLD}	Reflow soldering temperature [c]		260	°C

Notes:
a. In off-state, spike duty cycle D<0.01, spike duration <30μs.
b. For increased stability at high current operation, see Circuit Implementation on page 3
c. Reflow MSL3

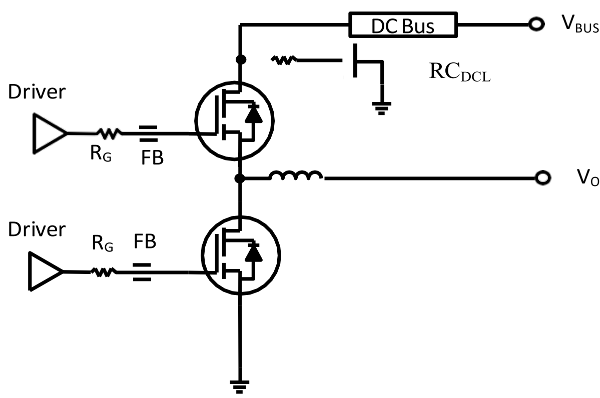


Thermal Resistance

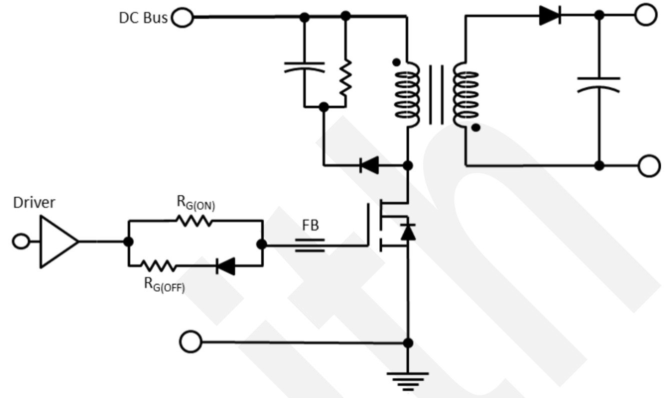
Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	5.5	°C/W
$R_{\Theta JA}$	Junction-to-ambient [d]	50	°C/W

Notes:
d. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper area and 70μm thickness)

Circuit Implementation



Simplified Half-bridge Schematic



Simplified Single Ended Schematic

Recommended gate drive: (0V, 8V) with $R_{G(tot)}$ = 30~60 Ω[a]

Recommended gate drive: (0V, 12V) with $R_{G(ON)}$ = 100 to 300 Ω
$R_{G(OFF)}$ = 0 to 15 Ω

Gate Ferrite Bead (FB1)	Required DC Link RC Snubber (RC_{DCL}) [b]
240Ω@100MHz	4.7-10nF + 5Ω

Notes:
a. For bridge topologies only. R_G could be much smaller in single ended topologies.
b. RC_{DCL} should be placed as close as possible to the drain pin.

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Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{DSS(BL)}$	Maximum drain-source voltage	650	—	—	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage	1.6	2.1	2.6	V	V_{DS}=V_{GS}, I_D=0.5mA
$R_{DS(on)eff}$	Drain-source on-resistance [a]	—	240	312	mΩ	V_{GS}=8V, I_D=5A
		—	492	—		V_{GS}=8V, I_D=5A, T_J=150°C
I_{DSS}	Drain-to-source leakage current	—	1.2	12	μA	V_{DS}=650V, V_{GS}=0V
		—	8	—		V_{DS}=650V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V_{GS}=20V
	Gate-to-source reverse leakage current	—	—	-100		V_{GS}=-20V
C_{ISS}	Input capacitance	—	760	—	pF	V_{GS}=0V, V_{DS}=400V, *f*=1MHz
C_{OSS}	Output capacitance	—	16	—		
C_{RSS}	Reverse transfer capacitance	—	2	—		
$C_{O(er)}$	Output capacitance, energy related [b]	—	24	—	pF	V_{GS}=0V, V_{DS}=0V to 400V
$C_{O(tr)}$	Output capacitance, time related [c]	—	47	—		
Q_G	Total gate charge	—	9.6	—	nC	V_{DS}=400V, V_{GS}=0V to 8V, I_D=4A
Q_{GS}	Gate-source charge	—	2.6	—		
Q_{GD}	Gate-drain charge	—	2.6	—		
Q_{OSS}	Output charge	—	19	—	nC	V_{GS}=0V, V_{DS}=0V to 400V
$t_{D(on)}$	Turn-on delay	—	19.4	—	ns	V_{DS}=400V, V_{GS}=0V to 8V, I_D=4A, R_G=30Ω, 4A driver
t_R	Rise time	—	3.4	—		
$t_{D(off)}$	Turn-off delay	—	53	—		
t_F	Fall time	—	10	—		

Notes:
a. Dynamic $R_{DS(on)}$ value; see Figures 18 and 19 for conditions
b. Equivalent capacitance to give same stored energy from 0V to 400V
c. Equivalent capacitance to give same charging time from 0V to 400V

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	3.7	A	V_{GS}=0V, T_C=100°C, ≤25% duty cycle
V_{SD}	Reverse voltage [a]	—	1.7	—	V	V_{GS}=0V, I_S=5A
		—	1.2	—		V_{GS}=0V, I_S=2A
t_{RR}	Reverse recovery time	—	16	—	ns	I_S=5A, V_{DD}=400V, di/dt=1000A/us
Q_{RR}	Reverse recovery charge	—	23	—	nC	

Notes:

a. Includes dynamic $R_{DS(on)}$ effect

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Typical Characteristics (T_C=25°C unless otherwise stated)

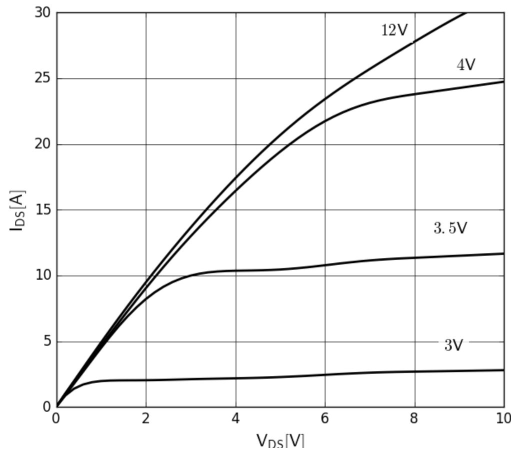

Figure 1. Typical Output Characteristics T_J=25°C
Parameter: V_{GS}

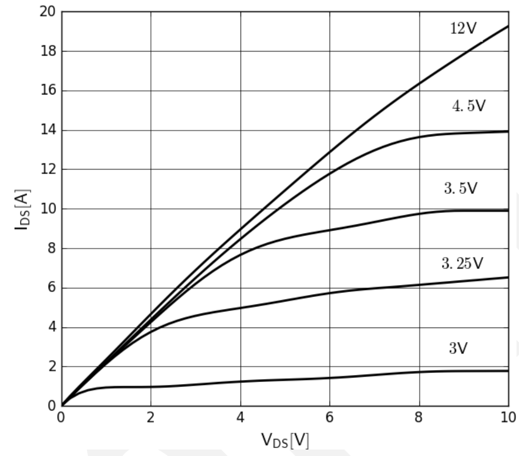

Figure 2. Typical Output Characteristics T_J=150°C
Parameter: V_{GS}

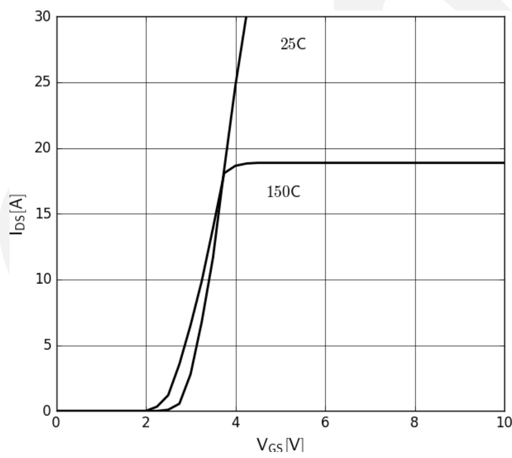

Figure 3. Typical Transfer Characteristics
V_{DS}=10V, parameter: T_J

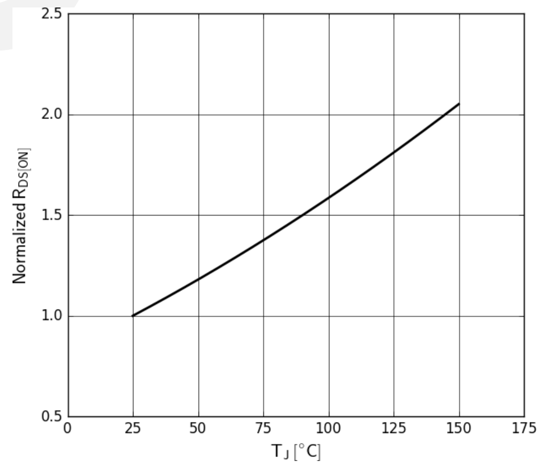

Figure 4. Normalized On-resistance
I_D=16A, V_{GS}=10V

Typical Characteristics (T_C=25°C unless otherwise stated)

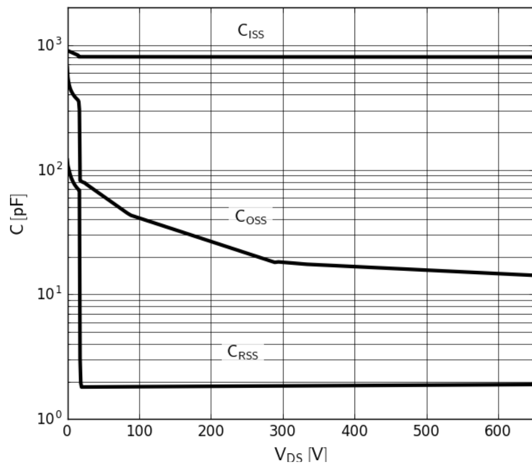

Figure 5. Typical Capacitance
V_{GS}=0V, f=1MHz

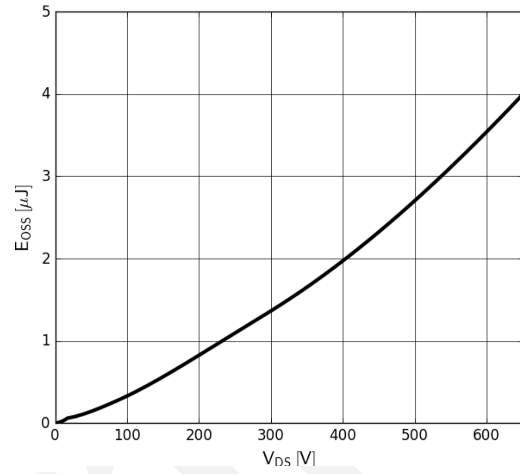

Figure 6. Typical C_{OSS} Stored Energy

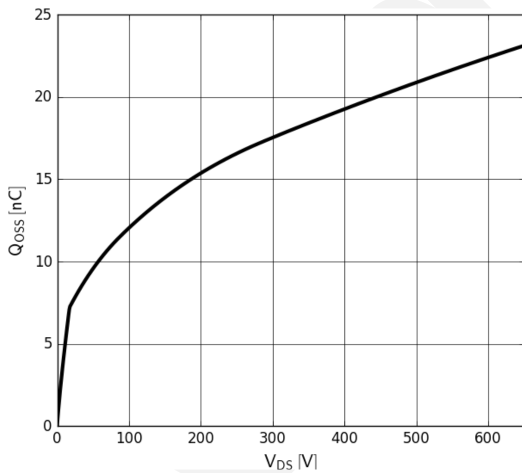

Figure 7. Typical Q_{OSS}

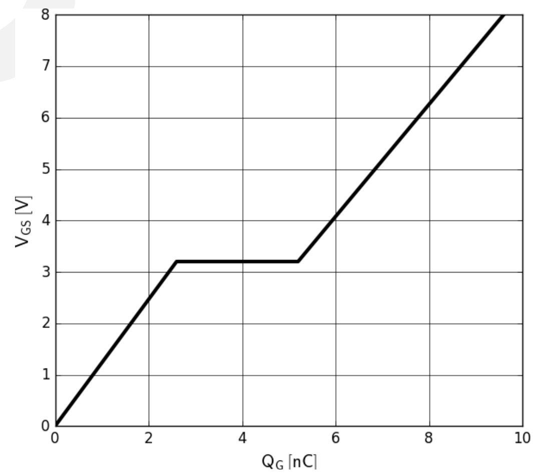

Figure 8. Typical Gate Charge
I_{DS}=4A, V_{DS}=400V

Typical Characteristics (T_C=25°C unless otherwise stated)

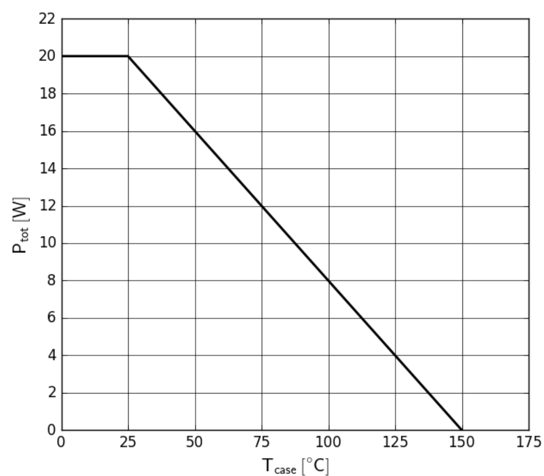

Figure 9. Power Dissipation

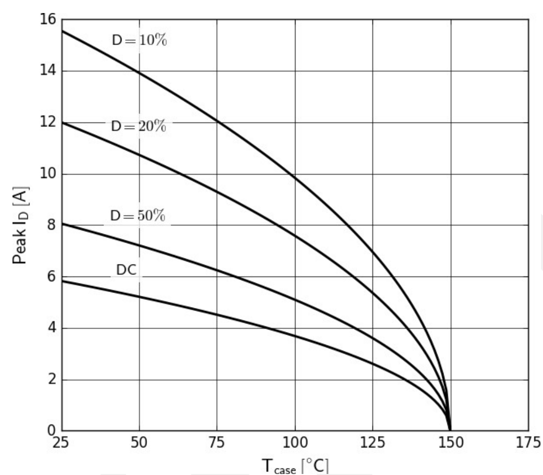

Figure 10. Current Derating
Pulse width ≤ 10μs, V_{GS} ≥ 10V

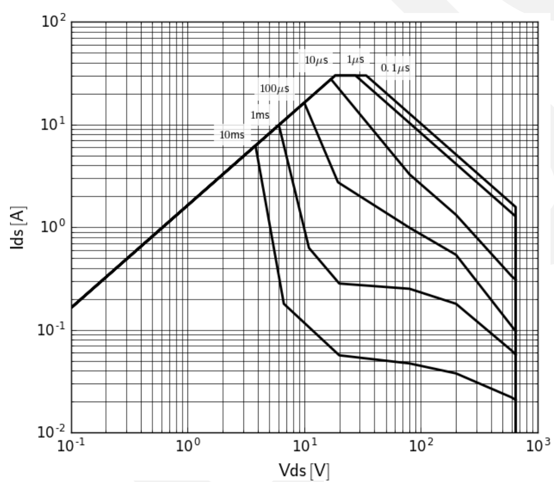

Figure 11. Safe Operating Area T_C=25°C

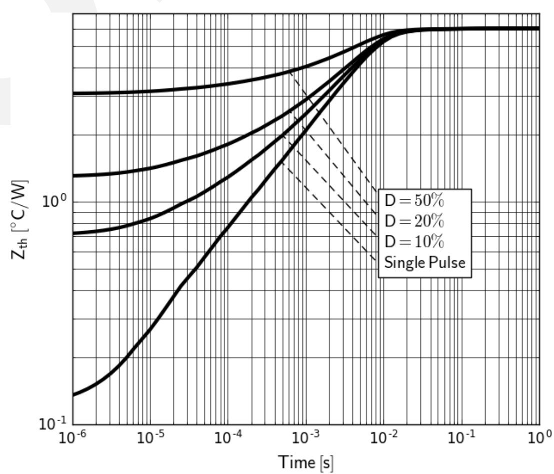

Figure 12. Transient Thermal Resistance

Typical Characteristics (T_C=25°C unless otherwise stated)

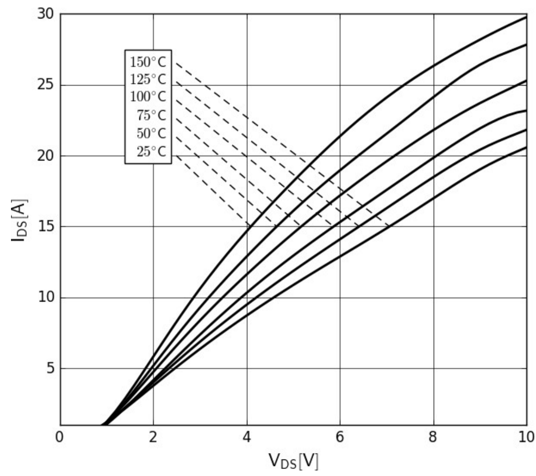

Figure 13. Forward Characteristics of Rev. Diode
I_S=f(V_{SD}), Parameter T_J

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Test Circuits and Waveforms

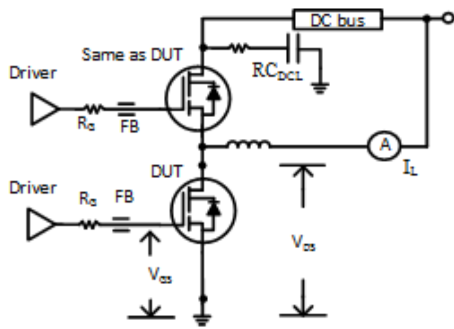

Figure 14. Switching Time Test Circuit (see circuit implementation on page 3 for methods to ensure clean switching)

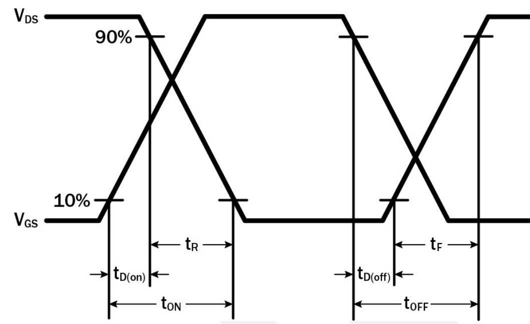

Figure 15. Switching Time Waveform

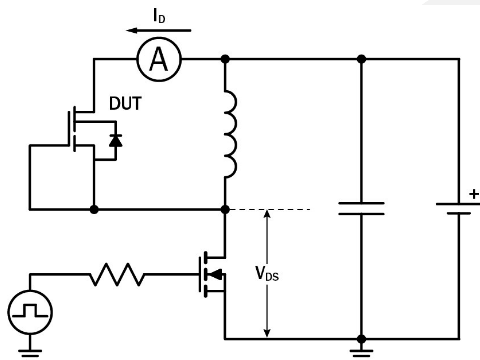

Figure 16. Diode Characteristics Test Circuit

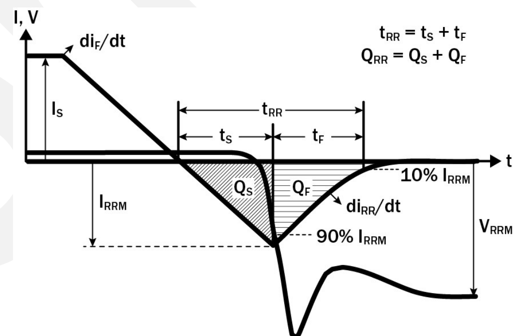

Figure 17. Diode Recovery Waveform

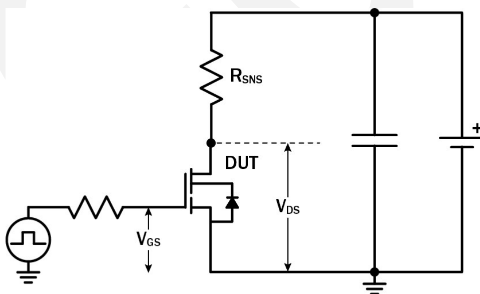

Figure 18. Dynamic $R_{DS(on)eff}$ Test Circuit

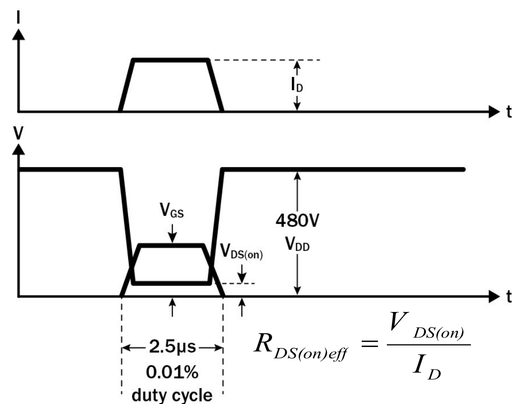

Figure 19. Dynamic $R_{DS(on)eff}$ Waveform

Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

The table below provides some practical rules that should be followed during the evaluation.

When Evaluating GS GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire

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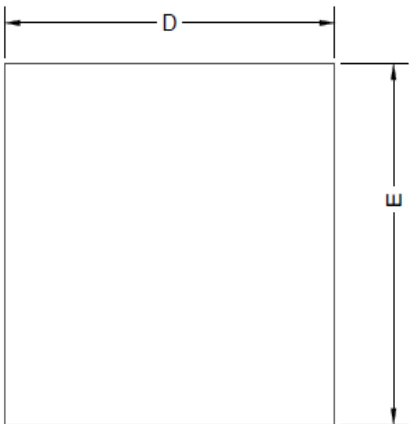
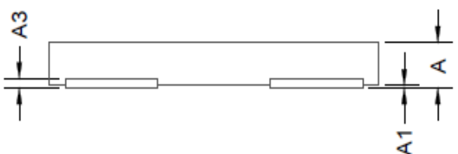
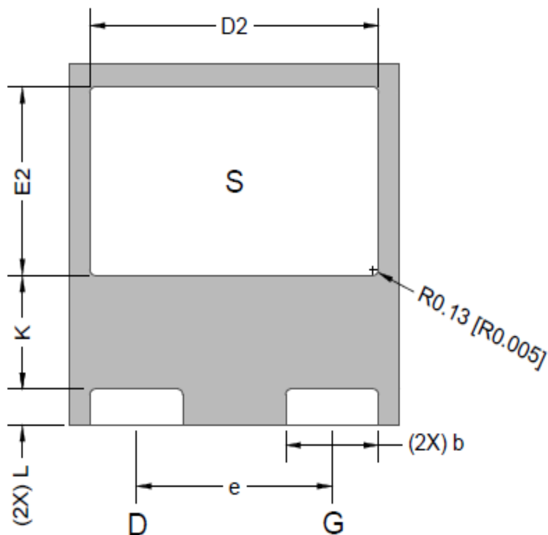
Mechanical







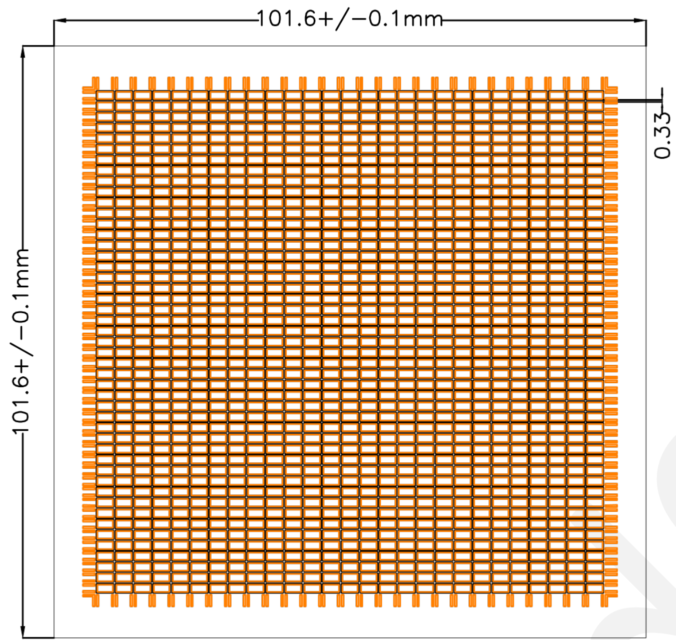
G: Gate
S: Source
D: Drain
Lead finish: Sn plating

DIM	mm			inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 REF.			0.007 BSC		
b	2.20	2.25	2.30	0.087	0.089	0.091
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	6.85	7.00	7.15	0.270	0.276	0.281
E	7.90	8.00	8.00	0.311	0.315	0.315
e	4.75 BSC			0.187 BSC		
E2	4.03	4.18	4.33	0.159	0.165	0.170
K	2.50	-	-	0.098	-	-
L	0.70	0.80	0.90	0.028	0.031	0.035

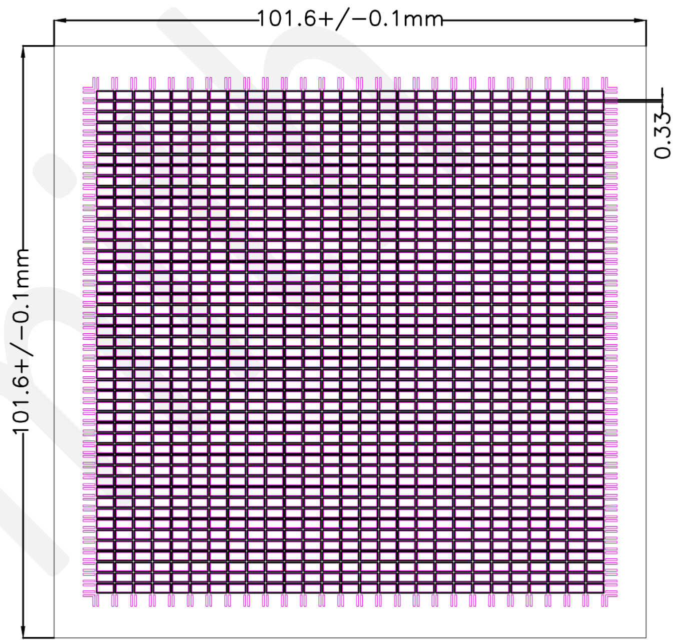
PQFN 8mmx8mm POD GS75H250G4LSG

INSTR

DPC TOP
Scale 1:1

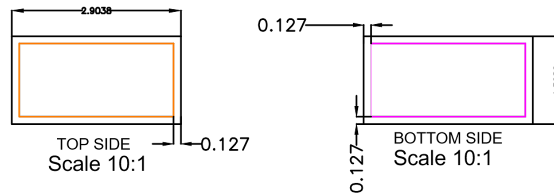


DPC BOTTOM
Scale 1:1



Notes:

1. Substrate: Al2O3, thickness 0.254 mm (0.010")
2. Saw street width: 0.330 mm (0.013")
3. Panel, size 101.6 mm x 101.6 mm, qty per panel = 47 x 27=1269 units.



GS75H250G4LSG Carrier ver. 1

UNLESS OTHERWISE SPECIFIED : DIMENSIONS ARE IN MM